We have multiple openings for Sr. Director of Design Engineering.

If you are interested in this job position, please send your resume to:

evelyn_hsiao@alchip.com

A candidate for a Sr. Director of Design Engineering is expected to:

- Manage the development of complex ASIC (Application Specific Integrated Circuits) designs of various applications, including tasks of chip-level floorplanning, placement and route (P&R), clock implementation, static timing analysis, and physical verification, using various design tools such as Synopsys, Cadence, or Siemens;
- Perform detailed calculations and develop cutting edge deep sub-micro design methodology and flow based on Synopsys/Cadence/Siemens design tools, particularly for low power and high performance design methodology and flow, which combines auto P&R and custom flow to meet extremely low power design spec;
- Coordinate with Electronic Design Automation (EDA) tool vendors to improve tool features and quality by testing the new features of tools with the company's internal designs of different applications, analyzing advantages and disadvantages regarding to compatibility, stability, and PPA (Performance Power and Area), and collecting issues and proposing new ideas and solutions;
- Work with the sales teams to explain the technical specifications of the ASIC designs, investigate any technical issues, estimate the die-size, floorplan, schedule, and resources needed, evaluate customer feedback, and recommend solutions to ensure that the designs meet customers' needs and specifications; and
- Work with the management to ensure that the design projects meet the company standards, and are completed on time and within budget.

Multiple positions are available.

Location of Employment

2107 N. First St., Suite 570, San Jose, CA 95131

Telecommuting one to two days per week is available.

Requirements

- Bachelor's degree in Electrical Engineering or related (foreign degree acceptable);
- 24 months of work experience in the offered position or related;
- 24 months of work experience in ASIC backend design using 7nm and below process technologies, including chip-level floorplanning, placement and route, clock

implementation, static timing analysis, and physical verification, using Synopsys, Cadence, or Siemens design tools;

- 24 months of work experience in low power design to minimize the power consumption of ASIC while maintaining high frequency spec, and while developing physical implementation flow that combines auto placement and route and custom flow to meet extremely low power design spec;
- 24 months of work experience in generating estimation for die-size, floorplan, schedule, and resources based on ASIC specifications from customers, and recommending solutions to specific technical problems to ensure that the designs meet customers' needs and specifications; and
- One to four months of travel to China twice a year.

Contact

- Alchip Technologies, Inc., Attn: Evelyn Hsiao, evelyn_hsiao@alchip.com