Alchip Technologies
IP Subsystem Services

August 2020

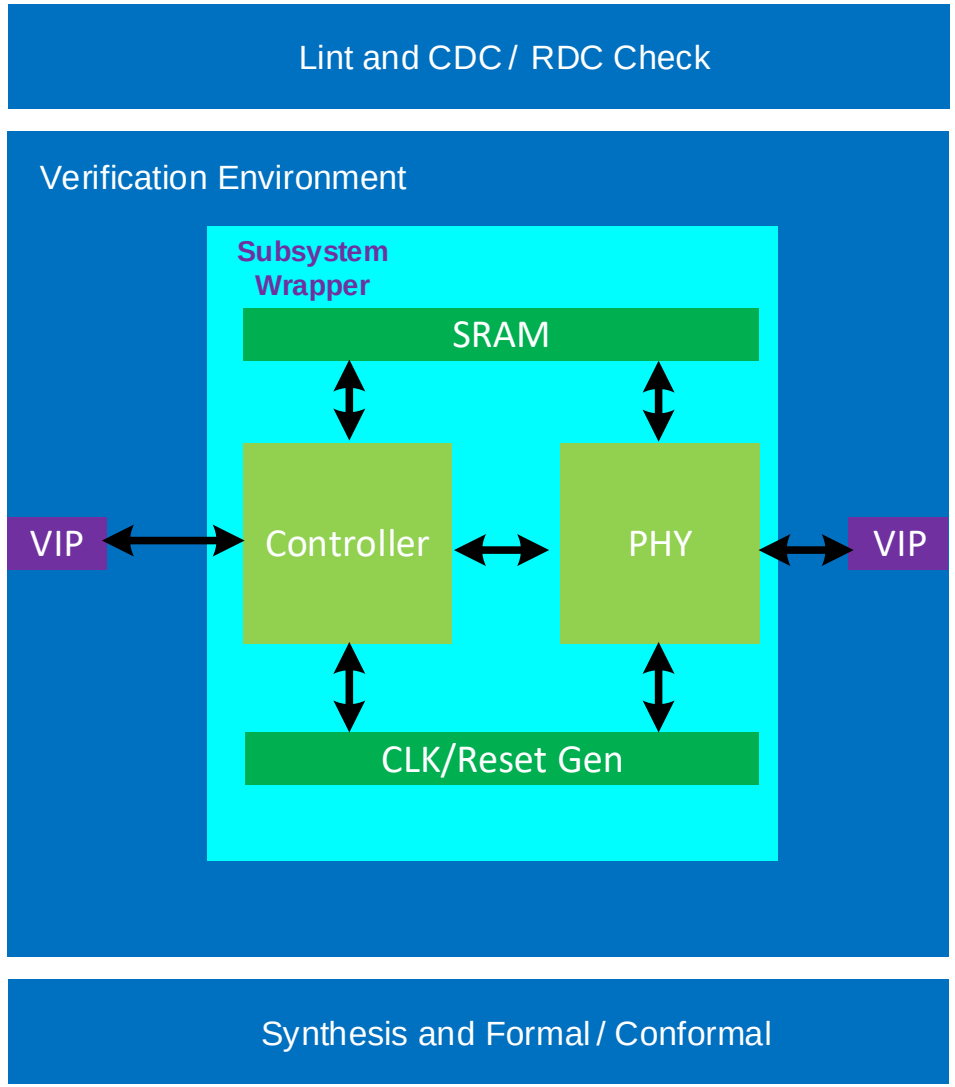
Silicon Heart of AI

IP Subsystem Service Scope

- IP Integration and Verification
- FPGA Prototyping and Emulation
- Software Driver Porting
- Chip Bring-up and Debug

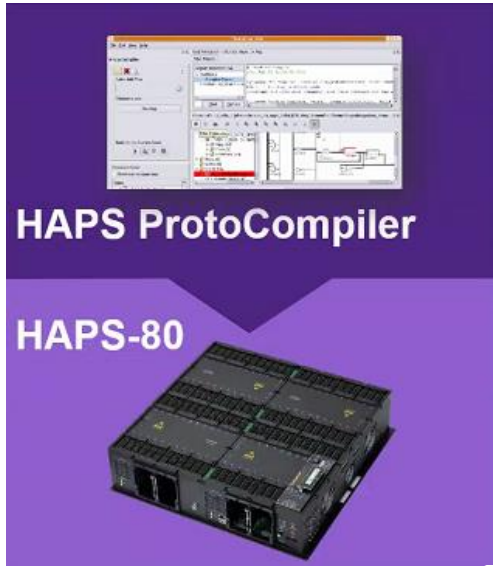
Interface IP Subsystem Integration

- Integration
  - Subsystem RTL Design
    - Controller/PHY connection
    - Clock/Reset gen
    - SRAM replacement
  - Front-end Flow
    - LINT/SDC/CDC check
    - SDC migration
    - Synthesis
    - Formal check
    - STA timing analysis
- Verification
  - IP level simulation
  - Subsystem level simulation
  - SoC level simulation
  - Netlist sim (pre- and post-)
- ES Bring up and Debug



FPGA Prototyping and Emulation

- FPGAs
  - Xilinx FPGAs for prototyping
  - Others for RTL verification and firmware ramp
- HAPS (Synopsys)
  - FPGA prototyping for function validation
  - HAPS-80 supports 26M ~ 1.6B ASIC gate capacity
  - Reduces time-to-peak performance prototyping to one month
  - Easy to use ProtoCompiler
- ZeBu (Synopsys)
  - SoC performance and power analysis
  - 150M ~ 9.6BG capacity
  - Virtual prototyping IP models (AMBA, DDR, PCIe…)
  - Porting analog/hard macro models
  - System level hardware/software emulation
  - Power/performance analysis



ZeBu Server 4

1.2BGates 2.4BGates

IP Integration Challenges

- Complicated protocol (PCIe, DDR…)
- High speed IP
- Error-prone
- Project scheduling bottleneck
- Time consuming chip bring up

Experienced Problem - Solving Team!

Alchip IP Integration Values

Why select Alchip's service for IP Integration?

- **Experienced team with broad IP familiarity**
  - Shorter TAT for IP/SoC integration
  - First time silicon success track record
  - 10+ IP integration/verification projects
  - Familiar with version differences
- **Collaborate with backend teams**
- **Close IP vendor relationship**
  - Highly efficient communication
  - Priority business and technical support

PCIe Subsystem Roadmap

- PCIe2 → PCIe3 → PCIe4 → PCIe5

- 2.5Gbps
- 1 lane
- 40nm
- Consumer

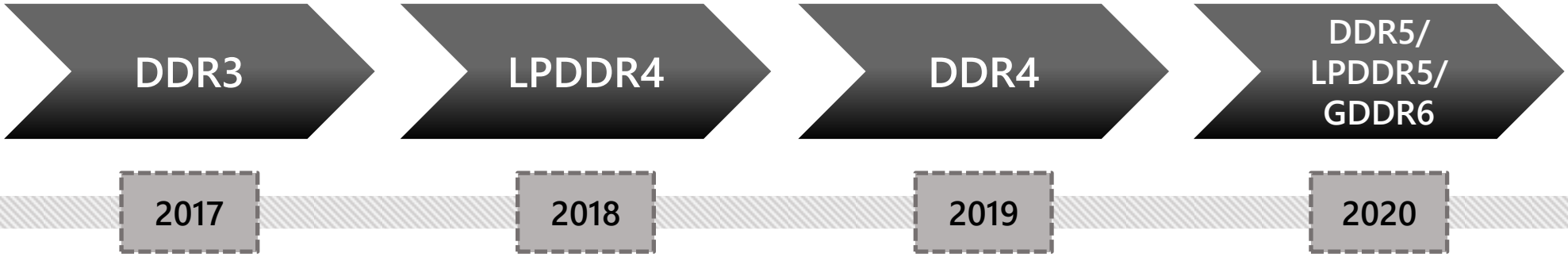
- 8Gbps
- 8 lanes
- 7nm
- AI

- 16Gbps
- 16 lanes
- 7nm
- AI/HPC

- 32Gbps
- 8 lanes
- 7nm
- AI

Memory Interface IP Subsystem Roadmap

- DDR3 → DDR4 → DDR5 *(plan)*
- LPDDR4 → LPDDR5 *(plan)*
- GDDR6 *(plan)*



- 1600Mbps
- 32bit
- 40nm
- Consumer

- 3200Mbps
- 32bit
- 12nm
- AI

- 3200Mbps
- 64+8 bit
- 7nm
- HPC

- 6400Mbps
- All new IP under evaluation

Summary

- Standard-setting PCIe and DDR subsystem service.
- Reliable, experienced engineering team.
- Proven successes.
- APLink 3.0 D2D IP ready year-end.
- HBM2E subsystem ready by year end.

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